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US-PAT-NO: 6601157
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TITLE: Register addressing

DATE-ISSUED: July 29, 2003

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FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
GB	0015092	June 20, 2000

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PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5390307	February 1995	Yoshida	712/225
☐	5390358	February 1995	Sugino	395/800
☐	5488730	January 1996	Brown, III et al.	395/800
☐	5924114	July 1999	Maruyama et al.	711/110
☐	5963746	October 1999	Barker et al.	712/20
☐	6205543	March 2001	Tremblay et al.	712/228
☐	6260137	July 2001	Fleck et al.	712/225
☐	6446190	September 2002	Barry et al.	712/24
☐	6487651	November 2002	Jackson et al.	712/13

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 380 849	August 1990	EP	
0 483 967	May 1992	EP	
0 483 967	May 1992	EP	

ART-UNIT: 2187

PRIMARY-EXAMINER: Yoo; Do Hyun

ASSISTANT-EXAMINER: Dinh; Ngoc V

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ABSTRACT:

There is disclosed a technique for accessing a register file which comprises defining a first register address as a plurality of bits and using said first register address to access said register file generating a second register address by using a sequence of said plurality of bits with at least one of said plurality of bits supplied via a unitary operator, the unitary operator being effective to selectively alter the logical value of said bit depending on its logical value in the first register address, and using said second register address to access said register file. A computer system for carrying out such a technique is also enclosed.

9 Claims, 7 Drawing figures

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Detailed Description Text (9):
Reverting to FIG. 4, the program memory 2 is connected to an instruction cache 3 which is connected to instruction fetch/decode circuitry 4. The fetch/decode circuitry issues addresses to the program memory and receives 64 bit lines from the program memory 2 (or cache 3), evaluates the opcode and transmits the respective instructions INST1, INST2 along X and Y channels 5.sub.x, 5.sub.y. Each channel comprises a SIMD execution unit 8.sub.x, 8.sub.y which includes three data processing units, MAC, INT and FPU and a load/store unit LSU 6. Each data processing unit MAC, INT and FPU and the load/store units LSU operate on a single instruction multiple data (SIMD) principle according to the SIMD lane expressed in the instruction according to the following protocol which defines the degree of packing of objects for packed data processing operations: (B)--8 bit objects (b.sub.0 . . . b.sub.7) (H)--16 bit objects (h.sub.0 . . . h.sub.3) (W)--32 bit objects (w.sub.0 . . . w.sub.1) (L)--64 bit objects (I) (S)--32 bit floating point (D)--64 bit floating point